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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,539	01/30/2002	Jung-Cheun Lien	ACT-317	3903

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

ARG

Office Action Summary	Application No.	Applicant(s)	
	10/066,539	LIEN ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 have been examined.

Claim Objections

2. Claim 5 is objected to because of the following informalities:

a. This claim is improperly depending on claim 2. For purpose of examination the Examiner is reading this claim to depend on claim 4.

b. In the limitation "...said horizontal tracks that turns all interconnect elements..." is missing the word "on" and should read, "...said horizontal tracks that turns on all interconnect elements..."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2-4:

These claims recite the limitation "in response to selected input stimuli". There is insufficient antecedent basis for "selected input stimuli" in these claims.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Abramovici et al. (US-6108806), hereinafter Abramovici.

Claim 1:

Abramovici teaches test pattern generators 20 which generate test patterns (defining a set of test inputs) that feed all blocks under test (BUTs) 22 in parallel via the global routing. Abramovici also teaches the disclosed testing method is particularly adapted to perform output response analysis by means of comparison with the expected response (determining/obtaining an expected output). Abramovici also teaches the third and seventh rows of programmable logic blocks (PLBs) in each FPGA being tested are initially configured as output response analyzers 24. Abramovici discloses each output response analyzer 24 compares two blocks under test 22 (comparing said expected results with said actual results) that receive test patterns from different test pattern generators 20. Abramovici further discloses each output response analyzer 24 compares corresponding outputs from 2 BUTs 22 to produce a local mismatch signal (LMN) which is ORed with the previous mismatch signal (PMN) from the previous output response analyzer to generate the output response analyzer mismatch (MM) (flagging an error). (Col. 5, lines 20-22, Col 6, lines 1-5, 17-23, 30, 31).

Claim 2 and 3:

Abramovici teaches that the FPGA logic is configured by loading configuration data (global control signal) from a test controller to establish a plurality of blocks under test (BTU), a first BTU (first set of tracks, per claim 2) and a second BTU (second set of tracks, per claim 3), which have separate test pattern generators 20 driving each one. Abramovici also teaches test pattern generators 20 which generate test patterns (plurality of signal sources) that feed all blocks under test (BUTs) 22 in parallel via the global routing. Abramovici further teaches the disclosed testing method is particularly adapted to perform output response analysis by means of comparison with the expected response. Abramovici also teaches the third and seventh rows of programmable logic blocks (PLBs) in each FPGA being tested are initially configured as output response analyzers 24. Abramovici discloses each output response analyzer 24 compares two blocks under test 22 (producing expected output values) that receive test patterns from different test pattern generators 20. Abramovici further discloses each output response analyzer 24 compares corresponding outputs from 2 BUTs 22 to produce a local mismatch signal (LMN) which is ORed with the previous mismatch signal (PMN) from the previous output response analyzer to generate the output response analyzer mismatch (MM) (flagging an error). (Col 4, lines 25-30, 44-55; Col. 5, lines 20-22; Col 6, lines 1-5, 17-23, 30, 31).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4 and 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Abramovici et al. (US-6108806), hereinafter Abramovici, in view of Wells et al. (US-6651238), hereinafter Wells.

Claim 4:

Abramovici teaches that the FPGA logic is configured by loading configuration data (global control signal) from a test controller to establish a plurality of blocks under test (BTU), a first BTU and a second BTU, which have separate test pattern generators 20 driving each one. Abramovici illustrates in FIG. 4a, the direction of the flow of test patterns is top to bottom (vertical tracks) and the extra PLBs in row R_5 are utilized as extra output response analyzers. Abramovici also teaches test pattern generators 20 which generate test patterns (plurality of signal sources) that feed all blocks under test (BUTs) 22 in parallel via the global routing. Abramovici further teaches the disclosed testing method is particularly adapted to perform output response analysis by means of comparison with the expected response. Abramovici also teaches the third and seventh rows of programmable logic blocks (PLBs) in each FPGA being tested are initially configured as output response analyzers 24. Abramovici discloses each output response analyzer 24 compares two blocks under test 22 (producing expected output values) that receive test patterns from different test pattern generators 20. Abramovici further discloses each output response analyzer 24 compares corresponding outputs from 2 BUTs 22 to produce a local mismatch signal (LMN) which is ORed with the

previous mismatch signal (PMN) from the previous output response analyzer to generate the output response analyzer mismatch (MM) (flagging an error). (Col 4, lines 25-30, 44-55; Col. 5, lines 20-22; Col 6, lines 1-5, 17-23, 30, 31, 46-52). Abramovici does not explicitly teach NOR and NAND circuits for producing expected output values. However, Abramovici does teach that each output response analyzer 24 compares corresponding outputs from 2 BUTs 22 to produce a local mismatch signal (LMN) which is ORed with the previous mismatch signal (PMN) from the previous output response analyzer to generate the output response analyzer mismatch (MM) (producing expected output). Wells teaches a logic gate tree that is formed of AND and OR gates to detect stuck-at-one faults and stuck-at-zero faults (produce expected results). Wells further suggest in another embodiment of the invention, other logic gates, such as NAND and NOR gates, replace the AND and OR gates in the logic gate tree designs. (Col. 2, lines 47-55; col. 14, lines 8-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Abramovici's OR circuit to incorporate Wells' NAND and NOR gates. The artisan would have been motivated to do so because this would enable Abramovici to detect stuck-at-one faults and stuck-at-zero faults rather than just stuck-at-zero faults.

Claim 5:

Abramovici teaches The floor plan for the second test session shown in FIG. 4b is obtained by flipping the floor plan for the test session shown in FIG. 4a around the horizontal axis (horizontal tracks) shown as a horizontal line between rows R_4, R_5 in the middle of the array. (Col. 6, lines 52-56).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cote et al. (US006725442)

Cote teaches interconnect verification in a FPGA (claim 1), using vertical and horizontal interconnect channels and AND/OR trees (claims 2-5).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gregory J. Lamarre
for
Albert DeCady
Primary Examiner

John J. Tabone, Jr.
Examiner
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JJT